ABSTRACT

Method and apparatus for determining power dissipation for an integrated circuit using computer simulation is described. More particularly, the integrated circuit is divided into cells, and one or more nodes are identified within each of the cells. A capacitive load value is ascribed to each of the nodes, and code is generated to track changes in state of each of the nodes. A total for changes in state for each node is divided by simulation time to determine a switching frequency. Using switching frequency, capacitive load and source voltage, dynamic power dissipation for each node may be determined. By summing dynamic power dissipation for all said nodes, total dynamic power dissipation may be determined.